AMENDMENTS TO THE SPECIFICATION

Replace the paragraph beginning at page 29, line 23 with:

When timing circuit 10 operates as described above, then transistor NT4 is turned on in response to the setting of the voltage level of node ~~NT1~~ N1 at 1 V, ground voltage GND is electrically coupled to node Nb, and the voltage level of node Nb is set at 0 V.

Replace the paragraph beginning at page 32, line 2 with:

Referring to Fig. 19, a driver circuit 620 according to the second modification of the sixth embodiment differs from driver circuit ~~610~~ 500 shown in Fig. 12 in that NAND circuit ND0 is deleted and transistors NT4 to NT6 are newly provided. In addition, NAND circuit ND1 and timing circuit 70 ~~constitutes~~ constitute a control circuit CT6a which controls the voltage levels of nodes N0 and N1. By way of example, it is assumed that transistors NT4 to NT6 are N-channel MOS transistors. It is also assumed that the current driving forces of transistors NT4 to NT6 are lower than that of transistor NT1. Specifically, it is assumed that the gate width of each of transistors NT4 and NT6 is smaller than that of transistor NT1.

Replace the paragraph beginning at page 32, line 12 with:

Transistor NT4 is arranged in parallel to transistor NT1, between node Nb and ground voltage GND, and the gate thereof is electrically coupled to node N1. Transistors NT5 and NT6 are connected in series between node N0 and ground voltage GND and the gates thereof receive input signals IN2 and IN1, respectively.

Replace the paragraph beginning at page 37, line 9 with:

Inverter INV4, which is connected ~~in series~~ to inverter INV1 through node Nb, is formed of transistors having a current driving force lower than that of inverter INV1. Specifically, inverter INV4 includes transistors PT4 and NT4.

Replace the paragraph beginning at page 37, line 32 with:

In a stationary state in which input signal IN is 0 V, node Nb is set at 0 V. Therefore, inverter 93 of control circuit 90 ~~is turned~~ turns on transistor 91 in response to the voltage level of node Nb. As a result, nodes N1 and N2 are electrically coupled to each other.

Replace the paragraph beginning at page 38, line 3 with:

At time T1, when input signal IN changes from 0 V to 1V, inverter 94 of control circuit 90 sets node N2 at 0 V. Accordingly, inverter INV1 ~~is turned~~ turns on transistor PTI in response to the voltage level of node N2 to thereby electrically couple power supply voltage VDD to node Nb. That is, the voltage level of node Nb is set at 1 V. In addition, as the voltage level of node Nb is set at 1 V, inverter 93 of control circuit 90 turns off transistor 91 and turns on transistor 92. Therefore, nodes N2 and N0 are electrically coupled to each other. Accordingly, the supply of voltage to node N1 is stopped and transistor PT1 is turned off.